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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,748	10/01/2004	Kiran V. Chatty	BUR920040050US1	5747

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EXAMINER
KITOV, ZEEV

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,748	CHATTY ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on January 20, 2006. Claim 4 is amended. Applicant Arguments are convincing and the Final Status is withdrawn. However, the search revealed a new ground for rejection. The Office Action follows.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "third nFET connected in series with the first nFET and the second nFET" recited in Claims 3 and 4 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Objection, 37 CFR 1.75(c)

Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. As a matter of fact, Claim 8 just repeats the same limitation as in Claim 7.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. A reason for that is in a following limitation: "a low frequency filter", which contradicts the Specification (Para 31, page 6) statement:

"the trigger circuit 44 is a high pass filter". For purpose of examination the trigger circuit was interpreted as a high pass filter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Andresen et al. (US 6,147,538). Regarding Claim 1, Andresen et al. disclose a transistor network connected between a voltage source and a ground (shown in Fig. 8), a bias network (R3a, R3b in Fig. 8) configured to bias a gate of a first transistor (N1b in Fig. 8) to a portion of a voltage value of the voltage source, and a trigger network (R1, P2, P1a, P1b in Fig. 8) communicating the occurrence of an electrostatic discharge to the gate of the second transistor (N1a in Fig. 3).

Regarding Claim 2, Andresen et al. disclose the first and the second n-FET devices connected in series (N1a, N1b in Fig. 8).

Regarding Claim 5, Andresen et al. disclose the voltage divider (R3a, R3b in Fig. 8) delivering a portion of the supply voltage to the gate of the first transistor (N1b in Fig. 8).

Regarding Claim 6, Andresen et al. disclose the resistor - capacitor circuit (R1, P2 in Fig. 8) filtering out non-electrostatic discharge events from the gate of the second transistor (N1a in Fig. 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen et al. As per Claim 3, it differs from Claim 2 rejected above by its limitation of a third n-FET being connected in series with the first and the second transistor supposedly the same way as other transistors. This limitation is addressed by the Court Decision *In re Harza,* 274 F.2d 669, 124 USPQ 378 (CCPA 1960). According to MPEP 2144.04(VI), the Court held that although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Andresen et al. solution by adding the third n-FET connected in series with two other n-FET's the same way as other transistors, because according to the Court Decision an by analogy, although the reference did not disclose the third transistor, mere duplication

of parts has no patentable significance unless a new and unexpected result is produced.

Regarding Claim 4, Andresen et al. disclose a transistor network connected between a voltage source and a ground (shown in Fig. 8), a bias network configured to bias a gate of a first transistor (N1b in Fig. 8) to a portion of a voltage value of the voltage source and a trigger network (R1, P1 in Fig. 8) communicating the occurrence of an electrostatic discharge to the gate of the second transistor (N1a in Fig. 8).

As to the third transistor connected in series with the first and the second transistor supposedly the same way as other transistors, this limitation is addressed above (see Claim 3 rejection).

Claims 7 – 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen et al. in view of Lin et al. (US 6,919,602). Regarding Claims 7 – 9, 12 - 15, Andresen et al. disclose an upper and lower nFET connected in series between a ground rail and a signal pad (813 in Fig. 8), a voltage divider (unidentified resistor, R3a, R3b in Fig. 8), a hi-pass filter (R1, P2) connected between the signal pad (813 in Fig. 8) and the gates of both the upper and the bottom nFET's (through R3a, R3b in Fig. 8) filtering out low frequencies. However, it does not disclose the clamp transistors and the RC filter being connected to the power supply rail. Lin et al. disclose the clamping transistor (N2 in Fig. 3) and the RC filter being connected to the power supply rail (A in Fig. 3). Both references have the same problem solving area, namely providing ESD protection. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to have modified the Andresen et al. solution by connecting the clamping transistors and the high-pass filter to the power supply rail according to teachings of Lin et al. rather than to the signal pin, because when protecting the circuit against ESD event on power supply rails the triggering of the clamping circuit should be initiated according to the ESD on the power supply rail and the clamping should be applied between the power supply rail and the ground, rather than between the ground and signal pad.

Regarding Claim 16, according to Andresen et al., configuring a gate of the upper transistor to be biased to a prescribed value inherently comprises applying a voltage to the power rail (Vdd in Fig. 8); otherwise there will be no bias for the gate.

Regarding Claim 17, according to Andresen et al., configuring a gate of the upper transistor to be biased to a prescribed value comprises attaching a bias network to the power rail (unidentified resistor, R3a, R3b connected to the power rail Vdd in Fig. 8) thus biasing a gate of the upper nFET (N1a in Fig. 8) to a prescribed value.

Regarding Claim 10, Andresen et al. disclose the voltage divider including resistors (R3a, R3b, in Fig. 8).

Regarding Claims 11 and 18, Andresen et al. disclose the high-pass filter communicating with a source and a drain of the lower nFET (N1b in Fig. 8); the high-pass filter is communicating with the source and drain of the lower nFET delivering the signal through transistors (P1a, P1b in Fig. 8) to the drain of the lower nFET and through additional resistor (R3b in Fig. 8) to the gate.

Regarding Claim 20, Andresen et al. disclose configuring the power supply rail to be in communication with a voltage source and the ground voltage (Vdd and ground in Fig. 8).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen et al. As per Claim 19, it differs from Claim 18 rejected above by its limitation of the time constant having specific value of one microsecond. The hi-pass filter is intended to filter out the low frequencies, therefore its time constant, which is associated with a cut-off frequency of the filter, is a result effective variable. Base on the Court Decision, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the time constant of the filter to a value of one microsecond, since it has been held that discovering an optimum value of the result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's Arguments have been given careful consideration but they are mostly moot in view of new grounds of rejection. The current Office Action maintains the objection to the Drawings, which Applicant has argued in the previous response dated July 1, 2005. The Applicant's Arguments was that it would be obvious to one of ordinary skill in the art to be able to utilize such a third nFET and an additional drawing is not necessary to facilitate the understanding of the invention. The US Patent Rules

paragraph 1.83(a) makes an explicit statement regarding content of the Drawings: "The drawing in a nonprovisional application must show every feature of the invention specified in the claims". Therefore the Argument is non-convincing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
2/20/2006

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